



# 1-Mbit (64K x 16) Static RAM

## Features

- **Temperature Range**
  - Automotive: -40°C to 125°C
- **High speed**
  - $t_{AA} = 15 \text{ ns}$
- **Optimized voltage range: 2.5V–2.7V**
- **Low active power: 360 mW (max.)**
- **Automatic power-down when deselected**
- **Independent control of upper and lower bits**
- **CMOS for optimum speed/power**
- **Package offered: 44-pin TSOP II**

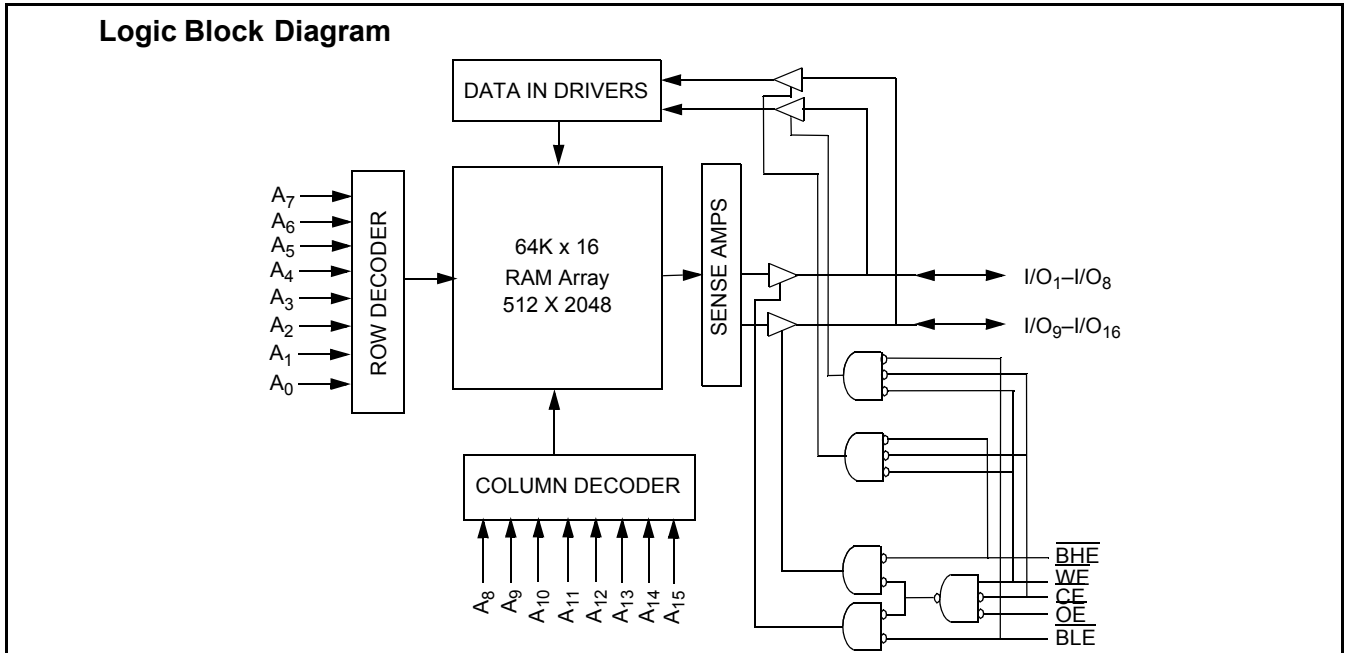
## Functional Description

The CY7C1021CV26 is a high-performance CMOS static RAM organized as 65,536 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_1$  through  $I/O_8$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_9$  through  $I/O_{16}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{15}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_1$  to  $I/O_8$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_9$  to  $I/O_{16}$ . See the truth table at the end of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_1$  through  $I/O_{16}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

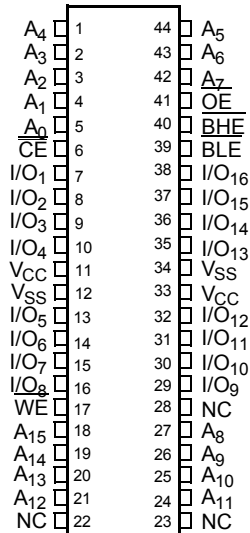


## Selection Guide

	CY7C1021CV26-15
Maximum Access Time (ns)	15
Maximum Operating Current (mA)	80
Maximum CMOS Standby Current (mA)	10

**Note:**

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = V_{CC(typ.)}$ ,  $T_A = 25^\circ\text{C}$ .

**Pin Configuration**
**TSOP II -Top View**

**Pin Definitions**

Pin Name	Pin Number	I/O Type	Description
A <sub>0</sub> -A <sub>15</sub>	1-5, 18-21, 24-27, 42-44	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>1</sub> -I/O <sub>16</sub>	7-10, 13-16, 29-32, 35-38	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
NC	22, 23, 28	No Connect	<b>No Connects.</b> This pin is not connected to the die.
WE	17	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a Write is conducted. When selected HIGH, a Read is conducted.
CE	6	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
BHE, BLE	39, 40	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> BLE controls I/O <sub>8</sub> -I/O <sub>1</sub> , BHE controls I/O <sub>16</sub> -I/O <sub>9</sub> .
OE	41	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins.
V <sub>SS</sub>	12, 34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	Power Supply	<b>Power Supply inputs to the device.</b>

**Note:**

2. NC pins are not connected on the die.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> to Relative GND<sup>[3]</sup> .... -0.5V to +4.6V  
 DC Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub>+0.5V

DC Input Voltage<sup>[3]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Automotive	-40°C to +125°C	2.5V-2.7V

**Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	CY7C1021CV26-15		Unit
			Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -1.0 mA	2.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 1.0 mA		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-3	+3	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-3	+3	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		80	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current — TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		15	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0		10	mA

**Capacitance<sup>[5]</sup>**

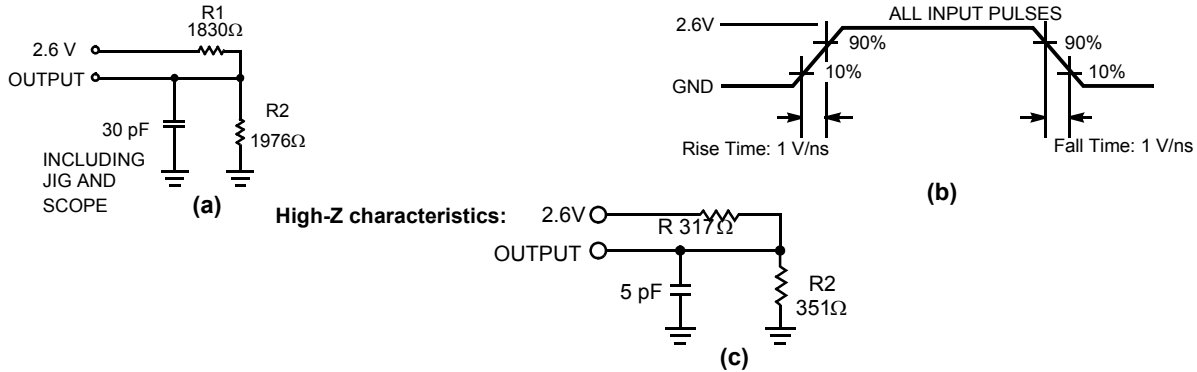
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 2.6V	8	pF
C <sub>OUT</sub>	Output Capacitance		8	pF

**Thermal Resistance<sup>[5]</sup>**

Parameter	Description	Test Conditions	44-lead TSOP-II	Unit
Θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) <sup>[5]</sup>	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	76.92	°C/W
Θ <sub>JC</sub>	Thermal Resistance (Junction to Case) <sup>[5]</sup>		15.86	°C/W

**Notes:**

- V<sub>IL</sub> (min.) = -2.0V and V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.5V for pulse durations of less than 20 ns.
- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms<sup>[6]</sup>**

**Switching Characteristics Over the Operating Range<sup>[7]</sup>**

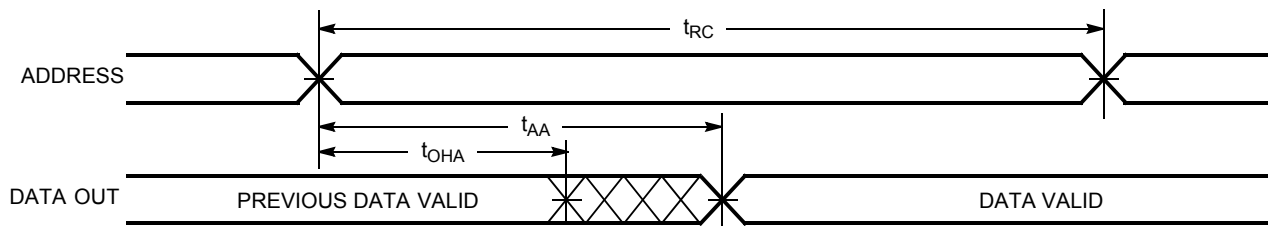
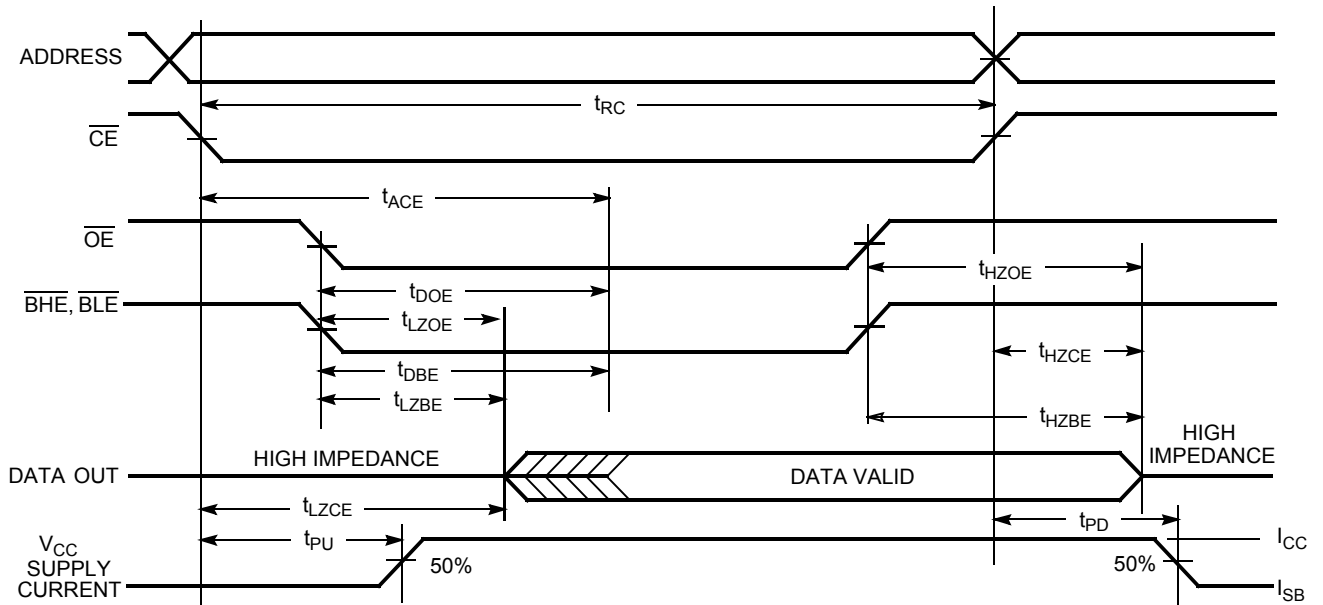
Parameter	Description	CY7C1021CV26-15		Unit
		Min.	Max.	
<b>Read Cycle</b>				
$t_{RC}$	Read Cycle Time	15		ns
$t_{AA}$	Address to Data Valid		15	ns
$t_{OHA}$	Data Hold from Address Change	3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		7	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z <sup>[8]</sup>	0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[8, 9]</sup>		7	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[8]</sup>	3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[8, 9]</sup>		7	ns
$t_{PU}^{[10]}$	$\overline{CE}$ LOW to Power-Up	0		ns
$t_{PD}^{[10]}$	$\overline{CE}$ HIGH to Power-Down		15	ns
$t_{DBE}$	Byte Enable to Data Valid		7	ns
$t_{LZBE}$	Byte Enable to Low-Z	0		ns
$t_{HZBE}$	Byte Disable to High-Z		7	ns
<b>Write Cycle<sup>[11]</sup></b>				
$t_{WC}$	Write Cycle Time	15		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10		ns
$t_{AW}$	Address Set-Up to Write End	10		ns
$t_{HA}$	Address Hold from Write End	0		ns
$t_{SA}$	Address Set-Up to Write Start	0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		ns
$t_{SD}$	Data Set-Up to Write End	8		ns
$t_{HD}$	Data Hold from Write End	0		ns

**Notes:**

- AC characteristics (except High-Z) are tested using the Thevenin load shown in Figure (a). High-Z characteristics are tested for all speeds using the test load shown in Figure (c).
- Test conditions assume signal transition time of 2.6 ns or less, timing reference levels of 1.3V, input pulse levels of 0 to 2.6V.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZBE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW,  $\overline{WE}$  LOW and  $\overline{BHE}/\overline{BLE}$  LOW.  $\overline{CE}$ ,  $\overline{WE}$  and  $\overline{BHE}/\overline{BLE}$  must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

**Switching Characteristics** Over the Operating Range<sup>[7]</sup> (continued)

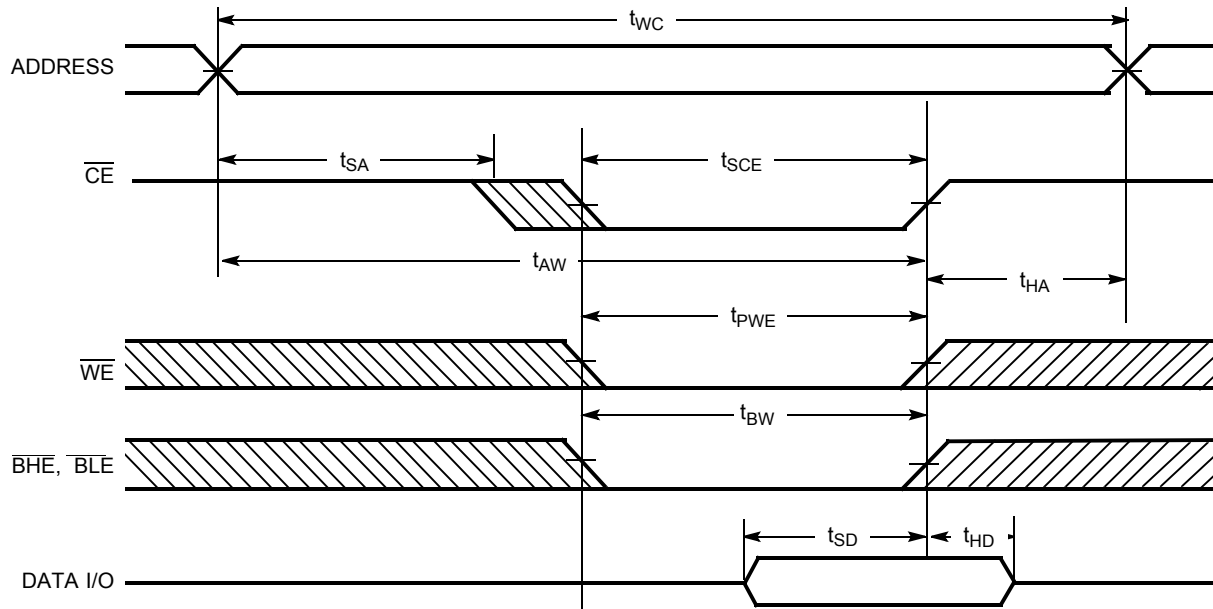
Parameter	Description	CY7C1021CV26-15		Unit
		Min.	Max.	
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>	3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[8, 9]</sup>		7	ns
$t_{BW}$	Byte Enable to End of Write	9		ns

**Switching Waveforms**
**Read Cycle No. 1**<sup>[12, 13]</sup>

**Read Cycle No. 2 (OE Controlled)**<sup>[13, 14]</sup>

**Notes:**

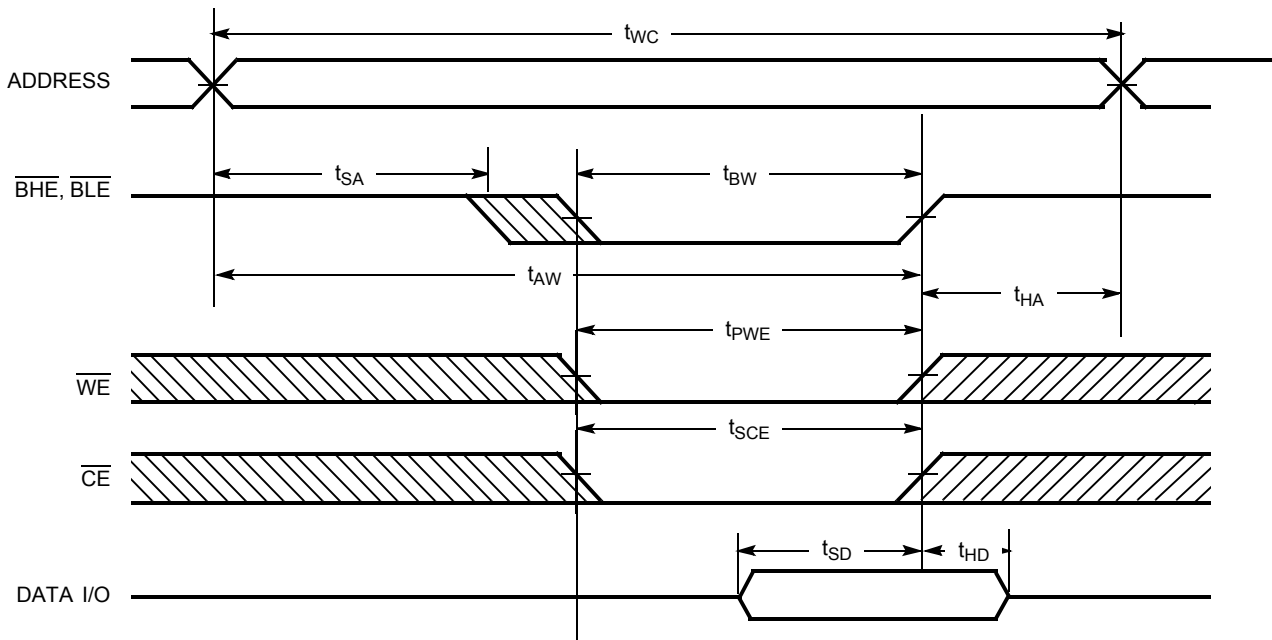
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ .
13.  $\overline{WE}$  is HIGH for Read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[15, 16]</sup>



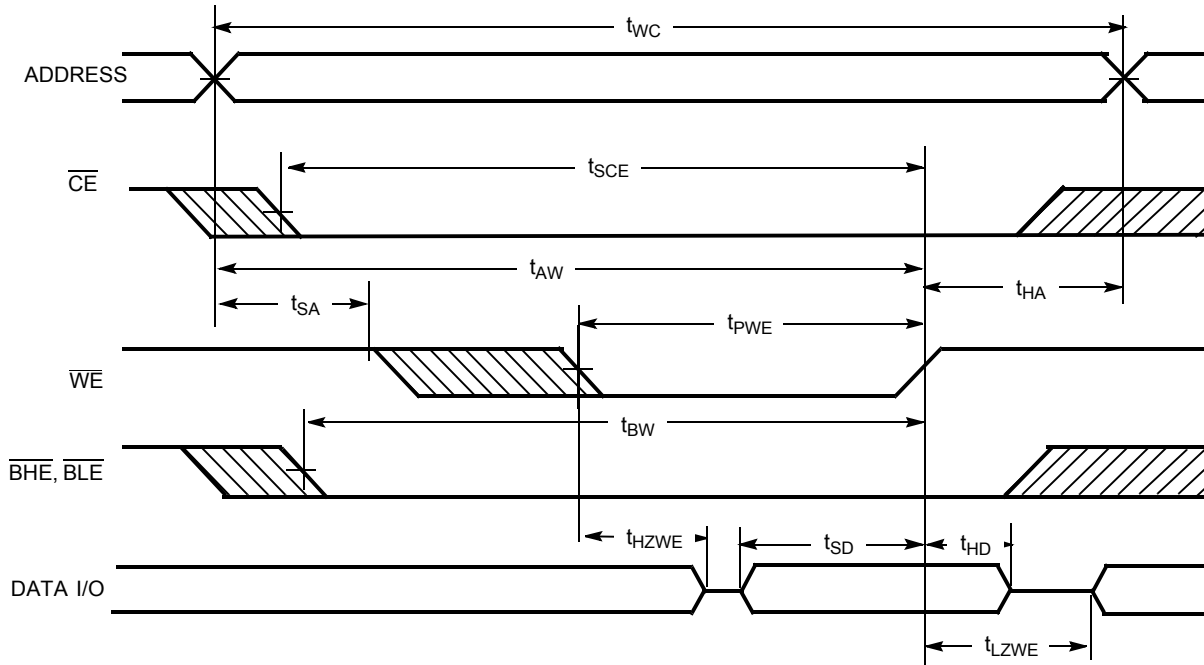
Write Cycle No. 2 ( $\overline{BLE}$  or  $\overline{BHE}$  Controlled)



Notes:

- 15. Data I/O is high-impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
- 16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms** (continued)

**Write Cycle No. 3 ( $\overline{WE}$  Controlled, LOW)**

**Truth Table**

CE	OE	WE	BLE	BHE	I/O <sub>1</sub> -I/O <sub>8</sub>	I/O <sub>9</sub> -I/O <sub>16</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read – All bits	Active ( $I_{CC}$ )
			L	H	Data Out	High-Z	Read – Lower bits only	Active ( $I_{CC}$ )
			H	L	High-Z	Data Out	Read – Upper bits only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write – All bits	Active ( $I_{CC}$ )
			L	H	Data In	High-Z	Write – Lower bits only	Active ( $I_{CC}$ )
			H	L	High-Z	Data In	Write – Upper bits only	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

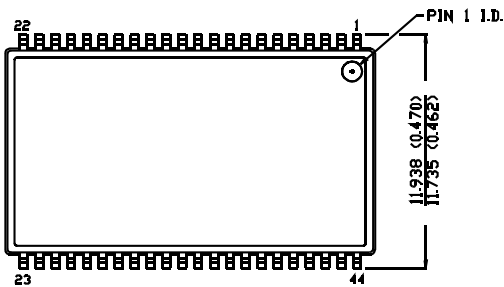
**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1021CV26-15ZE	Z44	44-lead TSOP Type II	Automotive

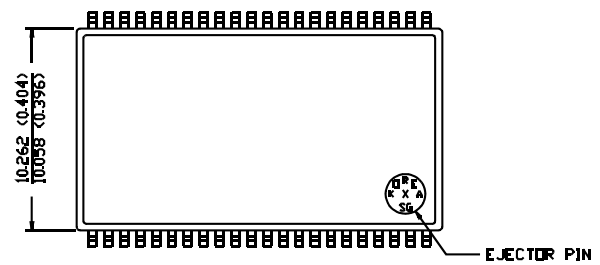
Package Diagrams

44-pin TSOP II Z44

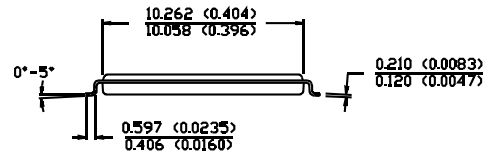
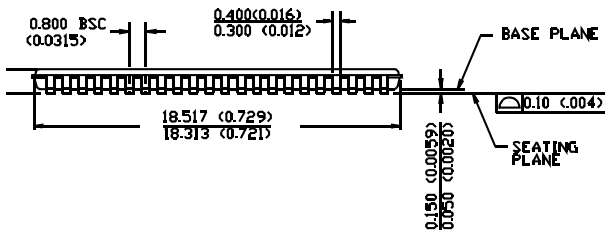
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



BOTTOM VIEW



51-85087-\*A

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**Document History Page**

<b>Document Title: CY7C1021CV26 1-Mbit (64K x 16) Static RAM</b> <b>Document Number: 38-05589</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	238454	See ECN	RKF	New datasheet for Automotive